A High Framerate Readout IC with in-Pixel ADC for X-Ray Detectors

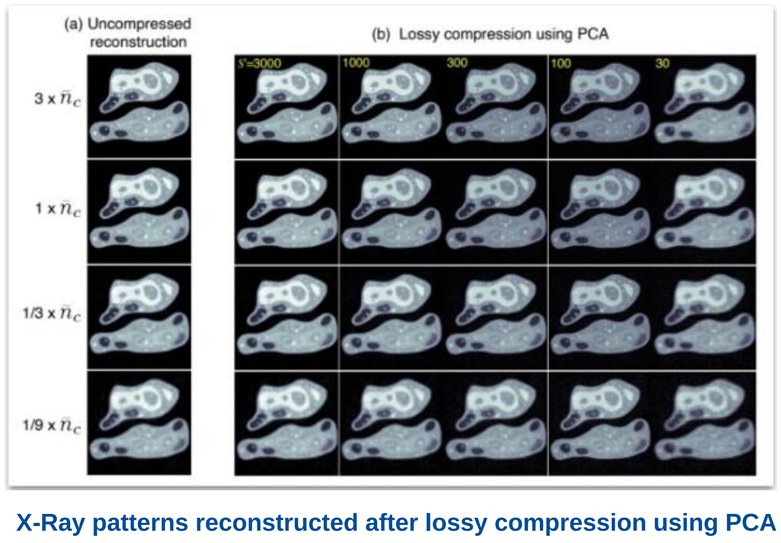
Troy England on behalf of Microelectronics Division

Fermi National Accelerator Laboratory, Batavia, Illinois, USA

High Frame Rate X-Ray Detectors

Large-area pixelated readout ICs for X-ray detectors at light sources have 200×200 pixels per chip, utilize 10-12b ADCs for digitizing data, and need to operate continuously without deadtime at high frame rates up to 1 Mfps, thus generating approximately ≥ 0.5 Tbps of data. The main bottleneck at this stage is the off-chip data transfer. If this data could be reduced by a factor between $50 \times$ and $100 \times$ then 1Mfps readout can be achieved with 2-4 multi-gigabit links.

Although front-end ROICs have adopted early digitization, such as in-pixel ADCs [2] and TDCs, they still rely on data transfer from pixel to the periphery, on-edge data serialization, and high-speed off-chip data transfer. The AI-in-Pixel ASIC distributes digital compression algorithms throughout the pixel array, enabling compression at the source rather than the periphery.

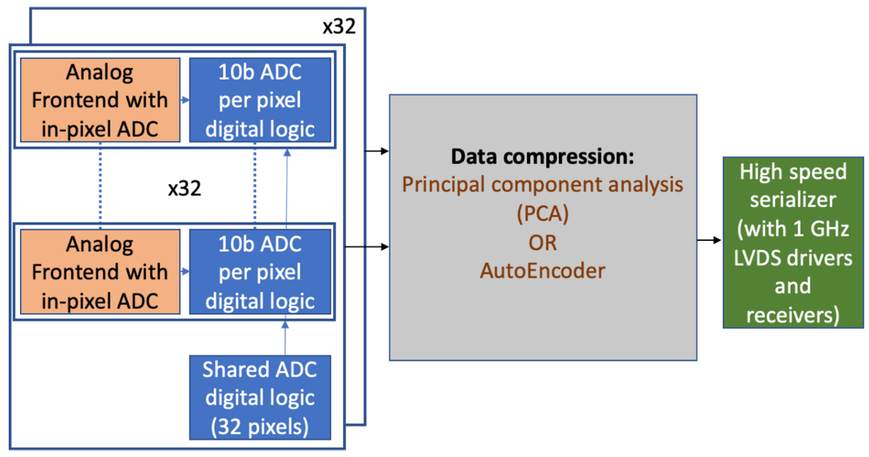


X-Ray patterns reconstructed after lossy compression using PCA

The AI-in-Pixel ASIC

The ASIC is composed of multiple "quadrants" with 32×32 ADC pixels embedded within distributed digital readout logic.

Each quadrant implements a different digital readout algorithm: As a baseline for comparison, the first AI-in-Pixel test chip implements full readout (no compression) and zero-suppression (ZS). Zero-suppression is not expected to be an effective algorithm because non-zero pixels may comprise > 40% of the array in noisy conditions. The second AI-in-Pixel test chip implements Principal Component Analysis (PCA) which achieves $50 \times$ compression, adds one clock cycle latency, and results in a 44% increase in the pixel area, as well as an AutoEncoder which achieves $70 \times$ compression, adds 30 clock cycle latency, and results in a 21% increase in pixel area. These algorithms provide a pathway to overcoming the I/O bottleneck while maintaining the accuracy needed for image reconstruction and further scientific analysis.

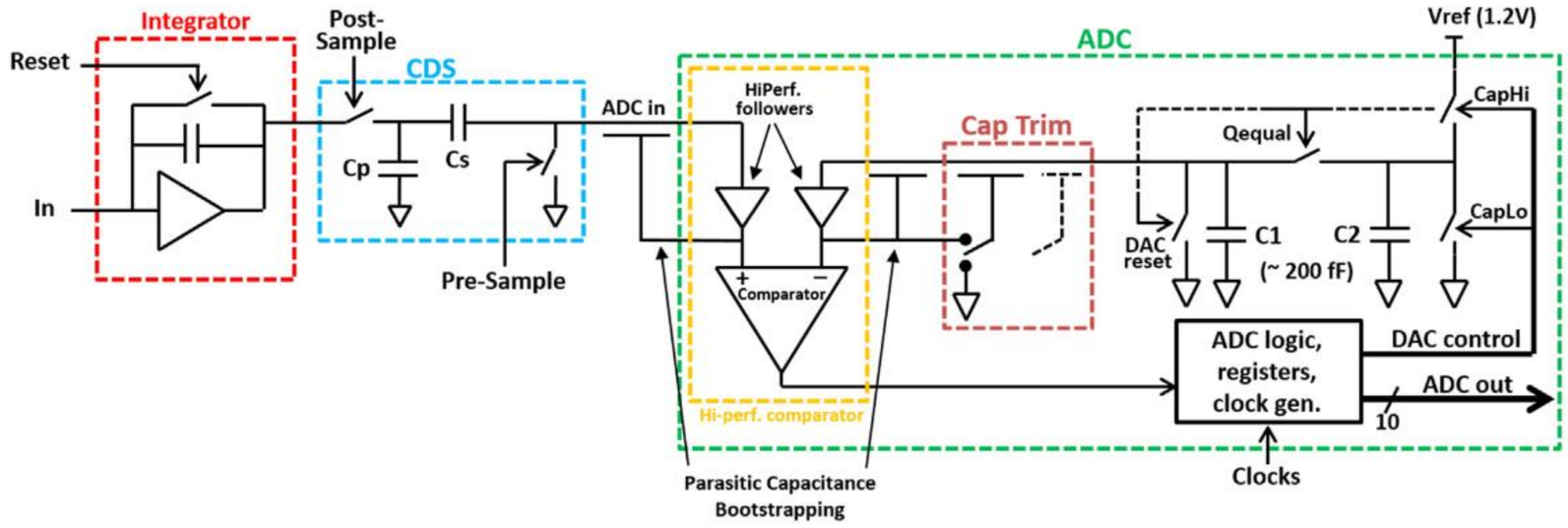


Block diagram of one AI-in-Pixel quadrant consisting of 1024 pixels.

Low-Noise Front End

The AI-in-Pixel ASIC contains a low-noise pixelated front end called the X-Ray Readout Circuit (XROCKET). An integrator collects the charge mode sample from a pinned photodiode in the sensor chip integrated heterogeneously with the readout ASIC.

Capacitors C_{samp} and C_{pre} perform correlated doubling-sampling (CDS), which is critical to zero the pedestal level of the photodiode and mitigate the low-frequency noise of the integrator.



Simplified schematic of the XROCKET front end with sub-blocks annotated.

Compact 100 KSps SAR ADC

The sampled voltage captured by the front end is digitized by a 10-bit SAR ADC (left).

To achieve 10-bit accuracy in a small footprint, only two capacitors are used, C_L and C_R, which are digitally trimmed to match. Precise voltage references are generated from this pair of capacitors by sequentially charging C_R to either ground ($h_n = 0$) or V_{ref} ($h_n = 1$) and then shorting the two capacitors together to redistribute charge. The final voltage after N phases is:

$$\sum_{n=1}^{N} \frac{V_{ref} h_n}{2^{N-n+1}}$$

A comparator generates this final voltage to the sampled input voltage, and the result determines bit *N* of the digital approximation.

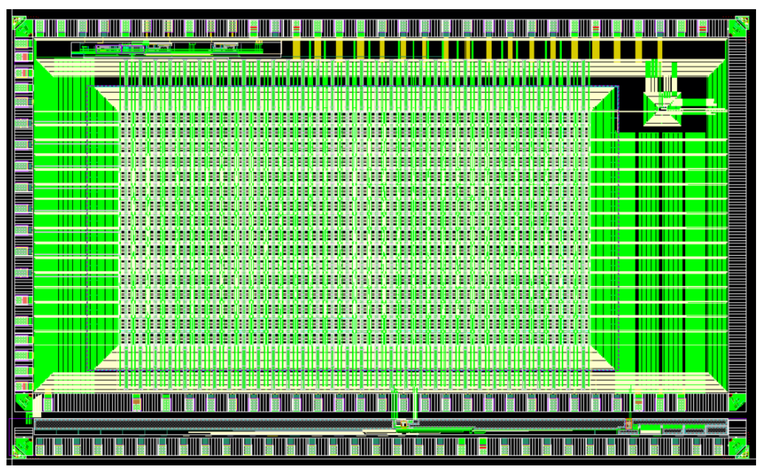
Future Work

Two test chips prototyping the quadrants described above were submitted in Sept and Dec 2022. Test results from these chips are expected in Spring 2023 to validate the implementation.

In Summer 2023, a new XROCKET front end will be co-designed with an AutoEncoder, trading lower resolution at digitization for an increased sample rate to allow the ASIC to achieve a sample rate of 1 Msps.

In future applications, the chip's compression algorithm can be developed to perform application-specific feature extraction.

Future efforts will expand the design to a reticle-sized array which can be vertically integrated with a co-designed sensor.



Layout capture of the Fall 2022 AI-in-Pixel test chip.

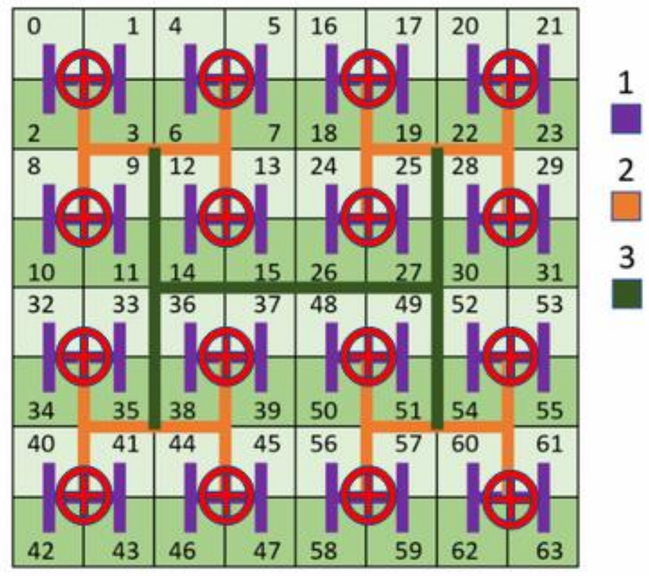


Diagram of the readout chip architecture, showing its H-tree structure as well as the multiply-accumulate units (red "+" signs) distributed throughout the array.

Further Reading

[1] F. Fahim et al., "A low-power, high-speed readout for pixel detectors based on an arbitration tree," IEEE Trans. VLSI Syst., vol. 28, no. 2, pp. 576–584, 2020.

[2] T. Zimmerman, G. Deptuch, and F. Fahim, "Compact, low power, high resolution adc per pixel for large area pixel detectors." U.S. Patent 11,108,981, issued August 31, 2021

In collaboration with Northwestern University

Contact: aquinn@fnal.gov, tengland@fnal.gov

Fermi National Accelerator Laboratory

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